In The Claims:

1. (Original) A DMOS device comprising:
a body of semiconductor material of a first conductivity type and a first doping level, said body having a surface;
a field region, of insulating material, extending along said surface and separating, in said body, at least one first active area and one second active area;
a first conductive region with said first conductivity type and a second doping level, higher than said first doping level, formed in said first active area;
a body region with a second conductivity type, formed in said second active area;
a second conductive region with said first conductivity type, formed in said body region;
at least one body-contact region, with said second conductivity type, formed inside said second conductive region and extending from said surface as far as said body region;
an insulating layer, extending on top of said surface and having a plurality of contact openings; and
a plurality of contacts of conductive material, extending in said contact openings as far as said first conductive region, said second conductive region and said body-contact region,
characterized in that said body-contact region is self-aligned to a respective contact.

2. (Original) The device according to claim 1, wherein said second conductive region comprises at least one first implanted region, having a third doping level lower than said second doping level, and two second implanted regions, having a fourth doping level higher than said third doping level, said first implanted region comprising a peripheral portion contiguous to said second implanted regions at least on one side facing said first conductive region and a transverse portion extending from said peripheral portion, physically separating and electrically connecting said second implanted regions; said transverse portion accommodating said body-contact region.

3. (Original) The device according to claim 2, further comprising:
a third active area separated from said second active area by said field region;

a third conductive region, formed in said third active area and having said first conductivity type and said second doping level;
a gate region, extending peripherally in part on top of said second active area and in part on top of said field region and having an internal peripheral edge; and
a spacing region, extending on top of said surface along said internal peripheral edge of said gate region;
wherein said peripheral portion of said first implanted region comprises two longitudinal portions extending underneath said spacing region, and said transverse portion extends between said longitudinal portions of said peripheral portion.

4. (currently Amended) The device according to ~~any one of the preceding claims~~claim 1, wherein said body-contact region has a greater depth than said second conductive region.

5. (Currently Amended) The device according to ~~any one of the preceding claims~~claim 1, wherein said first conductive region is a drain region and said second conductive region is a source region.

6. (Currently Amended) The device according to ~~any one of the preceding claims~~claim 1, wherein said first conductivity type of N and said second conductivity type is P.

7. (Original) A process for manufacturing a DMOS device comprising:
providing a body of semiconductor material having a surface, a first conductivity type, and a first doping level;
forming, along said surface, a field region of insulating material that separates, in said body, at least one first active area and one second active area;
forming, in said first active area, a first conductive region with said first conductivity type and with a second doping level, higher than said first doping level;
forming, in said second active area, a body region with a second conductivity type;
forming, in said body region, a second conductive region with said first conductivity type;

forming, inside said second conductive region, at least one body-contact region having said second conductivity type and extending from said surface as far as said body region;
forming, on top of said surface, an insulating layer;
forming a plurality of contact openings through said insulating layer; and
forming contacts of conductive material inside said contact openings;
characterized in that said step of forming a body-contact region is performed after said step of forming a plurality of contact openings and prior to said step of forming contacts so that said body-contact region is self-aligned to a respective contact.

8. (Original) The process according to claim 7, wherein said step of forming a body-contact region comprises forming a body-contact mask, which covers said insulating layer and said contact openings except where said body-contact region is to be formed, and implanting dopant agents determining said second conductivity type.

9. (Original) The process according to claim 7, further comprising introducing dopant ionic species of said second conductivity type at longitudinal ends of said body region prior to said step of forming a plurality of openings, and wherein said step of forming a plurality of openings comprises forming further contact openings above said longitudinal ends of said body region, and said step of forming a body-contact region moreover comprises forming further body-contact regions in said longitudinal ends of said body region.

l0. (Original) The process according to claim 7, wherein said step of forming a second conductive region comprises forming a first implanted region having a third doping level lower than said second doping level, and forming at least two second implanted regions, having a fourth doping level higher than said a third doping level, said step of forming a first implanted region comprising the step of forming a peripheral portion, contiguous to said first implanted regions at least on a side facing said first conductive region, and a transverse portion extending from said peripheral portion, physically separating and electrically connecting said first implanted regions and accommodating said body-contact region.

11. (Original) The process according to claim 10, comprising the steps of:
prior to said step of forming a body region, forming a gate region extending in part on top of said second active area and in part on top of said field region and having an internal peripheral edge;
after said step of forming a body region, implanting dopant species with said first conductivity type inside said body region, for forming a well with said first conductivity type and said third doping level;
forming a spacing region along said internal peripheral edge of said gate region;
selectively implanting dopant species of said first conductivity type inside said well thereby delimiting, in said well, said peripheral portion and said transverse portion, and forming said second implanted regions, said peripheral portion extending underneath said spacing region.

12. (Original) The process according to claim 11, wherein said step of forming a well comprises introducing dopant species in blanket mode inside said body region and said step of forming a body-contact region comprises implanting dopant species of said second conductivity type inside said transverse portion.

13. (Original) The process according to claim 11, wherein said step of forming a well comprises introducing dopant species inside said body region using a mask covering at least one central portion of said body region, so that said well has at least one non-implanted central portion, wherein said body region extends up to said surface and said step of forming a body-contact region comprises implanting dopant species with said second conductivity type inside said non-implanted central portion.

14. (Original) The process according to claim 7, wherein said step of forming a body-contact region comprises a superficial implanting and a deep implanting step.

15. (Original) The process according to claim 7, wherein said first conductivity type is N and said second conductivity type is P.

16. (Original) A DMOS device and the manufacturing process thereof, substantially as described herein with reference to the annexed figures.

17. (Original) A method of forming a DMOS device including a gate region, a drain region, a source body region, a body-contact region, and at least one contact, the method comprising:
forming a contact opening adjacent the body region;
after forming the contact opening, forming the body-contact region in the body region through the contact opening; and
after forming the body-contact region, forming a contact adjoining the body-contact region.

18. (Original) The method of claim 17 wherein forming the body-contact region comprises implanting a dopant having a conductivity type in the body region.

19. (Original) The method of claim 18 wherein the implanted dopant has a P+ type conductivity to form a P+ type body-contact region.

20. (Original) The method of claim 17 further comprising forming in the body region a second conductive region having a first conductivity type and wherein the body-contact region is formed within the second conductive region.

21. (Original) The method of claim 20 wherein the body region has a second conductivity type, wherein the body-contact region has the second conductivity type, and wherein the second conductive region has a first conductivity type.

22. (Original) A DMOS device, comprising:
a drain region;
a gate region;
a source body region;
a first conductive region in the body region;
a plurality of contacts of conductive material; and
a body-contact region in the first conductive region, the body-contact region being self-aligned with a respective one of the contacts.

23. (Original) The DMOS device of claim 22 further comprising:
a substrate of semiconductor material having a first conductivity type and having a

surface;
a field oxide region extending along the surface between the body region and the drain region; and
a second conductive region with the first conductivity type formed in the drain region.

24. (Original) The DMOS device of claim 23 wherein the first conductive region comprises a source region.

25. (Original) The DMOS device of claim 23 wherein the substrate, drain region, and first conductive region have the first conductivity type and wherein the body region and body contact region have the second conductivity type.

26. (Original) The DMOS device of claim 25 wherein the first conductivity type comprises N-type conductivity and the second conductivity type comprises P-type conductivity.

27. (Original) An electronic system, comprising:
an integrated circuit structure including a DMOS device, the DMOS device including,
a drain region;
a gate region;
a source body region;
a first conductive region in the body region;
a plurality of contacts of conductive material; and
a body-contact region in the first conductive region, the body-contact region being self-aligned with a respective one of the contacts.

28. (Original) The electronic system of claim 27 wherein the electronic system comprises a communications system.